ABSTRACT

The holding voltage (the minimum voltage required for operation) of a LVTSCR-like device is increased to a value that is greater than a dc bias on a to-be-protected node. The holding voltage is increased by reducing the size of the p+ emitter defined by the LVTSCR-like device. As a result, the LVTSCR can be utilized to provide ESD protection to power supply pins, having better current capabilities than a GGNMOS and better holding voltage characteristics than a LVTSCR.